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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,752	10/06/2003	Jeffrey H. Burns	DP-310264	2820

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EXAMINER	
CUTLER, ALBERT H	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,752	BURNS, JEFFREY H.	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/17/2005, 10/06/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to application 10/679,752 filed on October 6, 2003. Claims 1-19 are pending in the application and have been examined by the examiner.

Information Disclosure Statement

2. The Information Disclosure Statements (IDS) mailed on 10/06/2003 and 02/17/2005 were received and have been considered by the examiner.

Claim Objections

3. Claims 11, 12, 13, and 17 are objected to because of the following informalities: Lack of clarity and precision.

Consider claim 11, "at least one of said substrate **and** said optical material" should be written as "at least one of said substrate **or** said optical material" in order to preserve clarity and precision. Appropriate correction is required.

Consider claim 12, "at least one of a filter **and** antireflective material" should be written as "at least one of a filter **or** antireflective material" in order to preserve clarity and precision. Appropriate correction is required.

Consider claim 13, "at least one of embedded **and** dispersed" should be written as "at least one of embedded **or** dispersed" in order to preserve clarity and precision. Appropriate correction is required.

Consider claim 17, "at least one of a filter **and** an antireflective material" should be written as "at least one of a filter **or** an antireflective material" in order to preserve clarity and precision. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, 9-13, 15-17, and 19 rejected under 35 U.S.C. 102(e) as being anticipated by Melman et al.(US Patent 6,564,018).

Consider claim 1, Melman et al. teach:

An optical sensor circuit assembly(figures 1-9b), comprising:

an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49) including filter material(cover glass(106) has an antireflective coating(816) and

an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6);

and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c).

Consider claim 2, and as applied to claim 1 above, Melman et al. further teach that said filter material is embedded in said substrate("deposited on internal surface(818, i.e. embedded) of glass cover(806, i.e. said substrate)", column 7, lines 3-5).

Consider claim 3, and as applied to claim 1 above, Melman et al. further teach that said filter material is dispersed in said substrate("Instead of using the IR coating an IR absorbing glass may be used(i.e. the IR material is dispersed in the substrate)", column 7, lines 13-14).

Consider claim 4, and as applied to claim 1 above, Melman et al. further teach that said filter material comprises a thin film layer on said substrate(The Anti-reflective portion on the filter material(816) is applied as a coat(i.e. a thin film layer) on the surface of the substrate(806), column 6, lines 57-65).

Consider claim 5, and as applied to claim 4 above, Melman et al. further teach that said thin film layer(816) further comprises material having antireflective properties(column 6, lines 57-65).

Consider claim 6, and as applied to claim 1 above, Melman et al. further teach:

a circuit member("support element", 102, figure 8c) coupled to a first surface of said substrate(bottom surface, see figure 8c), said circuit member defining a plurality of electrically conductive leads(There are two conductive leads shown in figure 8c, The connection of these leads("wire", 112) is detailed in figures 5a and 5b, column 5, lines 54-61).

Consider claim 7, and as applied to claim 6 above, Melman et al. further teach:

said optical imaging element(116) includes an integrated circuit("semiconductor die" 116, column 5, line 46. The optical imaging element is in itself an integrated circuit.) and a plurality of electrically conductive pads("bonding pads", 512, figure 5b), said plurality of pads coupled with corresponding ones of said plurality of leads(112, see figure 5b, column 5, lines 54-61).

Consider claim 9, and as applied to claim 1 above, Melman et al. further teach:

at least one optical element("lens", 202, figure 3) positioned to direct electromagnetic radiation through said substrate and filter material and to said optical imaging element(see figure 3, column 4, lines 36-54).

Consider claim 10, and as applied to claim 9 above, Melman et al. further teach:

a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)) supporting said at least one optical element("lens", 202, figure 3) and coupled to a second surface(top surface, see figure 3)) of said substrate(Said substrate is labeled "106" in figure 3. Lens mount(300) is coupled to substrate(106) via film leads(302 and 304), column 4, lines 55-58.)

Consider claim 11, Melman et al. teach:

An optical sensor circuit assembly(figures 1-9b), comprising: an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49);

a thin film optical material coupled to said substrate(cover glass(106) has an antireflective coating(816, i.e. thin film), see figure 8b, column 6, line 57 through line 65);

an integrated circuit("semiconductor die" 116, column 5, line 46) having a face including an optical imaging element("sensor", 116, column 6, line 52, figure 8b), said face coupled with at least one of said substrate(The top face of optical imaging element(116) is coupled to substrate(806) with glue layer(800), see figure 8b).

Consider claim 12, and as applied to claim 11 above, Melman et al. further teach that said thin film optical material(816) comprises antireflective material(column 6, lines 57-65).

Consider claim 13, and as applied to claim 11 above, Melman et al. further teach:

said thin film optical material(816) comprises an antireflective material(see column 12 rationale); and

said optically transmissive substrate(806) comprises a filter material dispersed in said substrate("Instead of using the IR coating an IR absorbing glass may be used(i.e. a substrate with IR material dispersed within)", column 7, lines 13-14).

Consider claim 15, and as applied to claim 11 above, Melman et al. further teache:

at least one lens("lens", 202, figure 3) positioned to direct electromagnetic radiation through said substrate and filter material and to said optical imaging element(see figure 3, column 4, lines 36-54).

Consider claim 16, and as applied to claim 15 above, Melman et al. further teach:

a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)) supporting said at least one optical("lens", 202, figure 3) and coupled to a second surface(top surface, see figure 3)) of said substrate(Said substrate is labeled "106" in figure 3. Lens mount(300) is coupled to substrate(106) via film leads(302 and 304), column 4, lines 55-58.)

Consider claim 17, Melman et al. teach:

A method of assembling an optical sensor assembly, comprising the steps of: providing an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49);

associating at least one of a filter material and an antireflective material with the optically transmissive substrate(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6);

and coupling an integrated circuit("semiconductor die" 116, column 5, line 46) including an optical imaging element("sensor", 116, column 6, line 52, figure 8c) with the optically transmissive substrate(The top face of optical imaging element(116) is coupled to substrate(806) with glue layer(800), see figure 8b), and positioning the integrated circuit so that the optical imaging element faces the substrate(column 6, lines 48-51, see figure 8b, Light travels through the substrate and onto the sensor which is coupled to the substrate.).

Consider claim 19, and as applied to claim 17 above, Melman et al. further teach of coupling an optical element(lens, "202", see figure 3, column 4, lines 36-54), to the substrate using a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 8, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melman et al.(US Patent 6,564,018) in view of DiOrio et al.(US Patent Application Publication 2004/0217767).

Consider claim 8, and as applied to claim 7 above, Melman et al. teach of a plurality of leads and a plurality of pads(see claim 7 rationale). However, Melman et al. do not explicitly teach that a conductive bump is disposed between said plurality of leads and said plurality of pads.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board"

applications(paragraph 0029). Like Melman et al., DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. Melman teaches that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to connect the plurality of leads to the plurality of pads taught by Melman et al. with conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

Consider claim 14, and as applied to claim 11 above, Melman et al. further teach:

said integrated circuit("semiconductor die" 116, column 5, line 46) further comprises a plurality of electrically conductive pads("bonding pads", 512, figure 5b);

and said assembly further comprises: a circuit member("support element", 102, figure 8c) coupled to said substrate(see figure 8c), said circuit member(102) defining a plurality of electrically conductive leads(112, see figure 5b, column 5, lines 54-61).;

However, Melman et al. do not explicitly teach a plurality of conductive bumps disposed between said plurality of leads and said plurality of pads.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board" applications(paragraph 0029). Like Melman et al., DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. Melman teaches that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to connect the plurality of leads to the plurality of pads taught by Melman et al. with conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

Consider claim 18, and as applied to claim 17 above, Melman et al. further teach:

coupling a circuit member("support element", 102, figure 8c) to the substrate(The circuit member(102) is coupled to the bottom surface of the substrate(806) via the integrated circuit(116), see figure 8c); and

wherein the step of coupling an integrated circuit(116) with the optically transmissive substrate(806) includes coupling the optical imaging element(116) to the circuit member(102)(column 5, lines 54-61; see figures 5a and 5b).

However, Melman et al. do not explicitly teach that the coupling of the optical imaging element(116) to the circuit member(102) is done using conductive bumps.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board" applications(paragraph 0029). Like Melman et al., DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach

that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. Melman teaches that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to couple the optical imaging element(116) to the circuit member(102) taught by Melman et al. using conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER